



2823#

AMENDMENT TRANSMITTAL LETTER

Docket No.
T2171.0196

Application No.
09/873,580

Filing Date
June 4, 2001

Examiner
F. Toledo

Art Unit
2823

Applicant(s): Harumitsu Fujita et al.

Invention: MULTI-VOLTAGE LEVEL SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	10	- =		x	
Independent Claims	2	- =		x	
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					

☒ Large Entity

☐ Small Entity

☐ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. _____ in the amount of \$ _____.
A duplicate copy of this sheet is enclosed.

☐ A check in the amount of \$ _____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073
as described below. A duplicate copy of this sheet is enclosed.

☒ Credit any overpayment.

☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Michael J. Scheer

Dated: November 4, 2002

Michael J. Scheer
Attorney Reg. No. 34,425

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$ 400.00

Complete if Known

Application Number	09/873,580
Filing Date	June 4, 2001
First Named Inventor	Harumitsu Fujita et al.
Examiner Name	F. Toledo
Group Art Unit	2823
Attorney Docket No.	T2171.0196

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number

04-1073

Deposit Account Name

Dickstein Shapiro Morin & Oshinsky LLP

The Commissioner is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) (\$ 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
10	-31** = 0	x	= 0
Independent Claims	2	-3** =	=
Multiple Dependent		=	=

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee (\$)	Small Entity Fee Code	Small Entity Fee (\$)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	400.00
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(g)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR 1.129(a))	
149	740	249	370	For each additional invention to be	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 400.00

SUBMITTED BY

Name (Print/Type) Michael J. Scher

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34,425

Complete (if applicable)

Telephone (212) 835-1400

Signature

Michael J. Scher

Date

November 4, 2002



Docket No.: T2171.0196
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Harumitsu Fujita

Application No.: 09/873,580

Filed: June 4, 2001

For: MULTI-VOLTAGE LEVEL
SEMICONDUCTOR DEVICE AND ITS
MANUFACTURE

Group Art Unit: 2823

Examiner: F. Toledo

TECHNOLOGY CENTER 2800

#8/B
Amended
J. Hamilton
NOV - 7 2002
RECEIVED
11/12/02

AMENDMENT

Box Non-Fee Amendment
Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action mailed June 5, 2002, please amend the above-identified U.S. patent application as follows:

In the Claims:

Cancel claims 1, 2, 5 and 6.

1. (New) A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

providing a semiconductor substrate having at least first and second active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto at least said first and second active regions;

forming an electrode layer onto said gate oxide layer;